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SILICON CAPACITOR

SAMSUNG
ELECTRO-MECHANICS

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Interactive User Guide

Click ‘HOME,’ ‘CONTENTS,’ OR ‘GO BACK TO PAGE’ as needed, and it is also possible to ‘PRINT’ the pages.

If you click the icon at the top of the page, it is possible to view a specific page of choice.

By clicking this icon, you can jump directly to the cover page of this catalog.

By clicking this icon, you can jump directly to the Table of Contents.

By clicking this icon, you can jump directly to the previous page.

By clicking this icon, you can set and print pages of your choice.

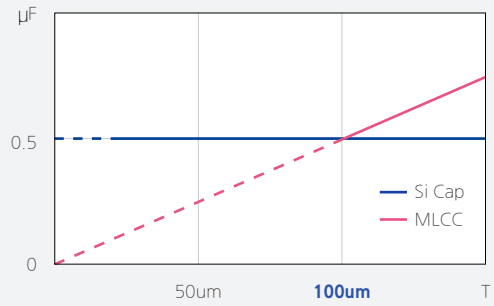
Contents

Explanation of Silicon Capacitors

- Manufactured by silicon-based semiconductor processes.
- Customized design and manufacturing based on customer requirements (capacitance, thickness, number of terminals, size, etc.).
- Beneficial for low ESL (Equivalent Series Inductance) implementation. The thickness can be made thin, and the capacitance variation rate is low under voltage and temperature changes.

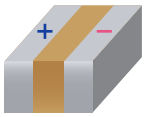
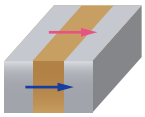
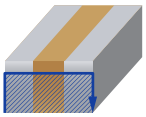
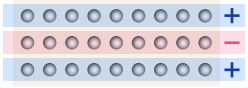
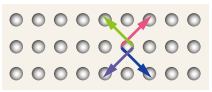
· Thin form factor

The wafer grinding process enables the thickness of the silicon body to be reduced to less than 100 μm.



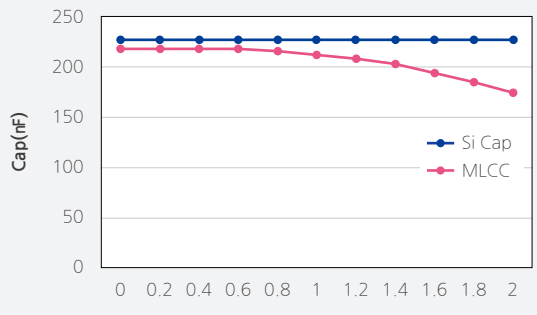
· Low ESL

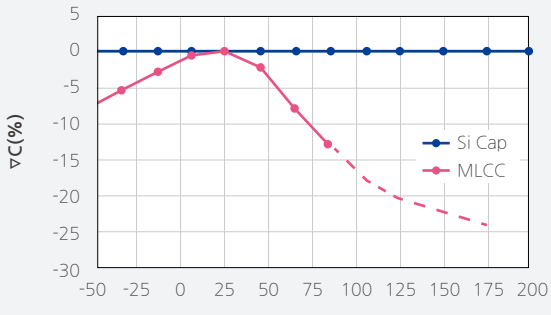
Based on customer requirements, the number and arrangement of terminals can be optimized. This allows for the cancellation of magnetic flux, reduction of current loops, and implementation of Low ESL.

Item	Structure	ESL	Magnetic Flux Cancellation	Current Loop
MLCC		60~80pH		
Silicon Capacitor		2↓		

· Low capacitance change rate

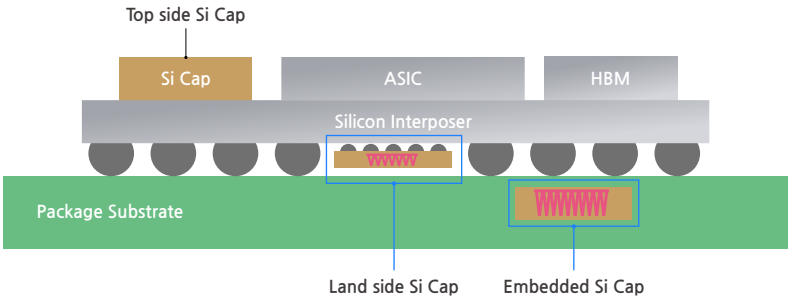
Silicon capacitors have low capacitance change rate with DC-bias and temperature changes due to the properties of the dielectric material.





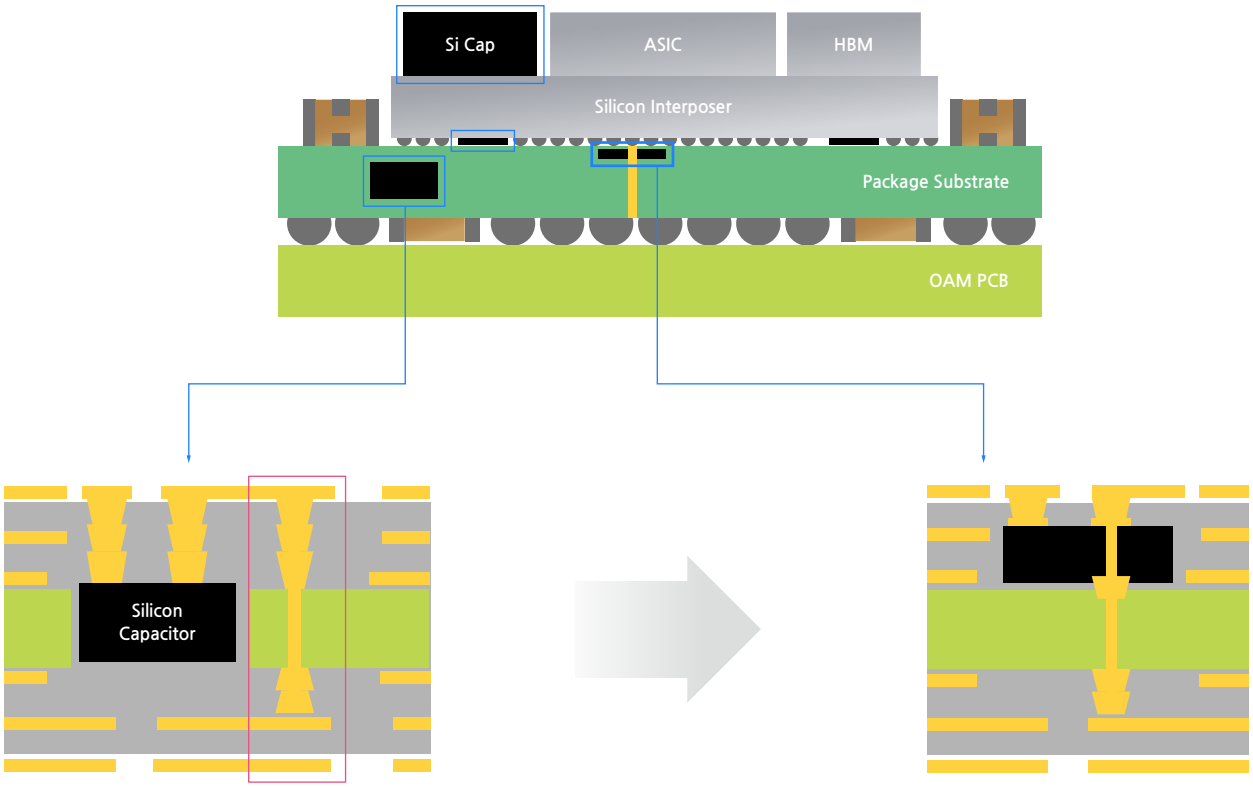
Explanation of Silicon Capacitors

- The package type and thickness of the Silicon capacitor are determined by the mounting location.
  - · **Land-side Silicon capacitors:** Mounted on the bottom of the silicon interposer.
  - · **Top-side Silicon capacitors:** Mounted on the side of the GPU, CPU, or ASIC.
  - · **Embedded Silicon capacitors:** Embedded inside the package substrate.



*** Embedded Silicon capacitor with TSV (through silicon via) in the build-up layer.**

: The Silicon capacitor and power pass-through can be integrated into a single die, and it can be embedded in the build-up layer to maximize its performance. This significantly improves routing efficiency, eliminating the need for additional power rails or split cavities.



Need additional route
to pass power to back side

Power pass thru
TSV → bottom bump on Si Cap

Application Guide

- Silicon capacitors were first adopted in high-performance application processors that require large capacitance and low ESL, and demand is increasing as the performance of chipsets for AI servers and automotive ADAS continues to improve.

	IT (AP)	Industry (AI server)	Automotive
Trend	high-performance, highly integrated AP	GPU performance improvement and high-speed signal connectivity with HBM	Advanced ADAS(Lv.4↑) and improved Processor performance.
Needs	thin form-factor, Low ESL, size reduction	ultra-high capacitance, Low ESL	high capacitance, Low ESL, High voltage High reliability (AEC-Q100 certification)
Size	1.2×1.0mm↓	Various Size by customer (1×1mm↓, Array-Type etc. Customized)	Various Size by customer (0.6×0.6mm↑, Customized)
Cap. Density	2~3uF/㎟	2~3uF/㎟	0.5uF/㎟↑
ESL/ESR	2pH↓/4mΩ	3pH↓/5mΩ	3pH↓/5mΩ
Voltage	1.35V	1.35V~1.8V	1.35~2.5V
Thickness * Si-body	70um (LSC type) 700~800um (Embedded)	70um (LSC/DSC type) 700~800um (Embedded)	50~70um (LSC/DSC type) * Land Side Capacitor/ Die side Capacitor
PKG type	LSC(PCB), Embedded	LSC/DSC(PCB), Embedded	LSC (PCB, Si-interposer)/DSC Wire bonding/Cu Pillar

Characteristics Performance

■ Specifications can be modified according to customer requirements.

Symbol	Parameter	Conditions	Unit	Spec
C	Capacitance Value	@25℃	nF	*Customized*
ΔCp	Capacitance Tolerance	@25℃	%	±20
T_{op}	Operating Temperature		℃	-40 ~ 125
T_{STG}	Storage Temperature		℃	-55 ~ 150
ΔC_T	Capacitance Temperature Variation	-40℃ ~ 125℃	ppm/℃	1000
RV_{DC}	Rated Voltage		VDC	*Customized*
BDV	Breakdown Voltage	@25℃	VDC	*Customized*
ΔC_{RVDC}	DC Capacitance Voltage Variation	0V ~ RV_{DC}, @25℃	%/VDC	10
IR	Insulation Resistance	RV_{DC}, @25℃, 120s	GΩ	10
ESR	Equivalent Series Resistance	@25℃, SRF	mΩ	TBD
ESL	Equivalent Series Inductance	@25℃, 1GHz	pH	TBD

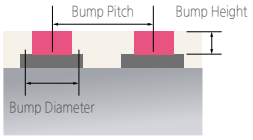
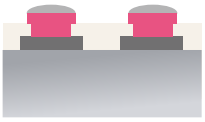
Product Lineup

Size [㎜]	Si thickness [㎛]	Capacitance [nF]	Power rails [ea]	Rated Voltage [V]	BDV [V]	PKG	Pad size [㎛]
1.26×1.03	68	2,600	4	1.35	4.0	LSC	60
	68	3,000	4	1.2	3.7	LSC	60
	68	550	4	2.5	8.0	LSC	60
	68	1,000	4	1.35	4.0	LSC	60
	70	512	4	1.35	4.0	LSC	60
1.26×0.51	70	256	2	1.35	4.0	LSC	60
0.96×0.88	60	1,050	2	1.35	4.0	LSC	55
11.01×8.35	750	103,950	198	1.35	4.0	DSC	55
2.00×2.00	738	8,800	2	1.2	4.0	Embedded	200
4.06×2.00	738	17,600	4	1.2	4.0	Embedded	200
4.02×4.02	738	35,000	4	1.2	4.0	Embedded	200

Pad and Bump Specifications

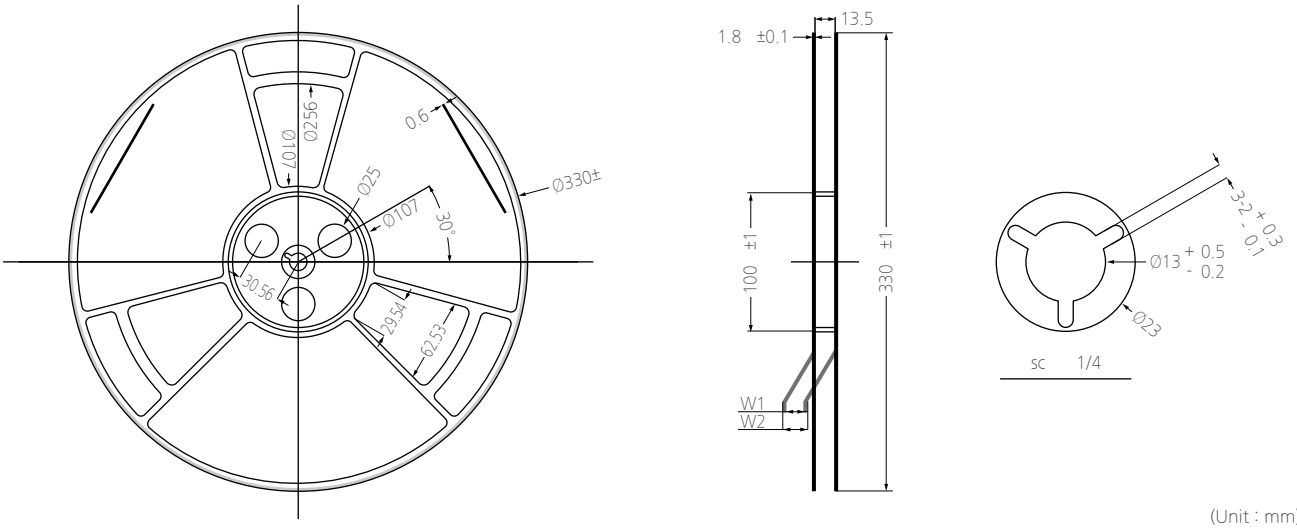
■ Support customized design (SMD, Embedded, Wire bonding)

· Bump dimension (If not included in the design rule guide, consultation is required)

Specifications		Embedded type	SMD type	Wire bonding
Min. Pitch	70μm			
Min. Diameter	45μm			
Height	10μm	Cu Pad	Cu Pillar Bump	Au/Al Pad

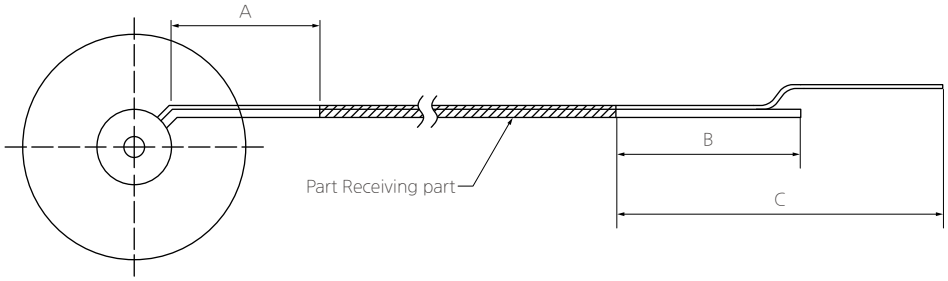
Packaging Specifications

1 Lok Reel Size



(Unit : mm)

Tape Width	Outer Diameter	Inner Diameter	W1	W2	Hall Pitch	Hall Diameter
8	330 (13")	100	9.5	13.5	30.56	Φ25

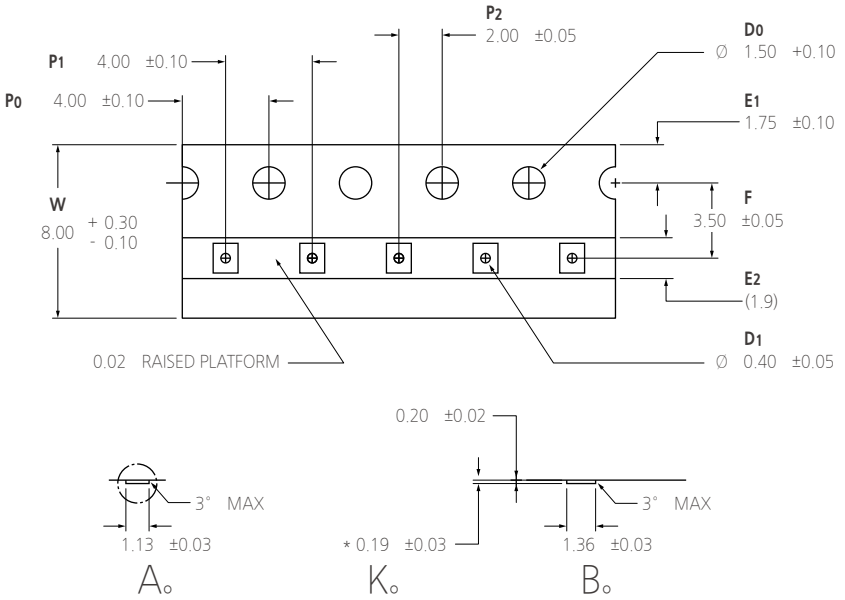


(Unit : mm)

A	B	C
1.2±0.1	1.2±0.1	1.5±0.1

Packaging Specifications

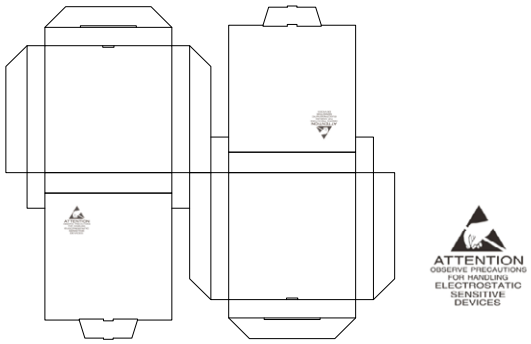
2 Tape Size

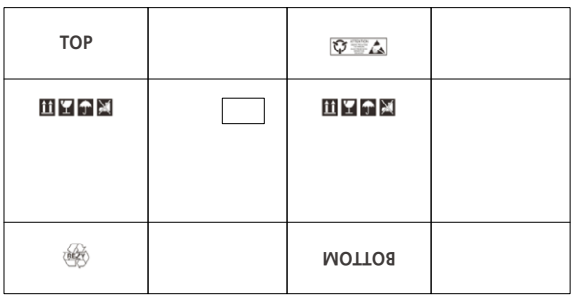


(Unit : mm)

Cavity dimension			W	P0	P1	P2	D0	D1	E1	E2	F
A0	B0	K0									
1.13±0.03	1.36±0.03	0.19±0.03	8+0.3/-0.1	4±0.1	4±0.1	2±0.05	Φ1.5±0.1	Φ0.4±0.05	1.75±0.1	(1.9)	3.5±0.05

3 Box Size





(Unit : mm)

Inner Box (13" × 1 Reel)		
Width	Depth	Height
350	347	50

(Unit : mm)

Out Box (13" × 6 Inner Box)		
Width	Depth	Height
380	370	375

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