



SILICON CAPACITOR

Interactive User Guide

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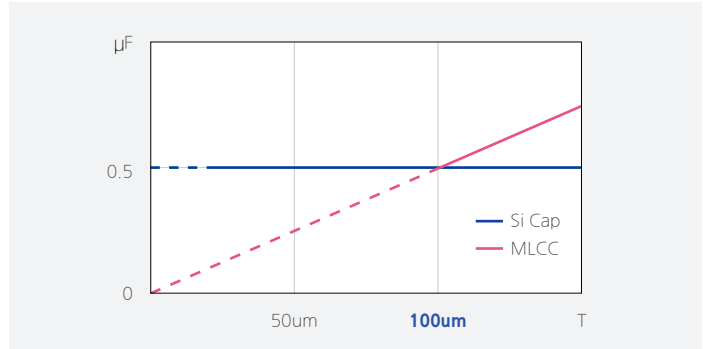
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Explanation of Silicon Capacitors

- Manufactured by silicon-based semiconductor processes.
- Customized design and manufacturing based on customer requirements (capacitance, thickness, number of terminals, size, etc.).
- Beneficial for low ESL (Equivalent Series Inductance) implementation. The thickness can be made thin, and the capacitance variation rate is low under voltage and temperature changes.

· **Thin form factor**

The wafer grinding process enables the thickness of the silicon body to be reduced to less than 100 μm .



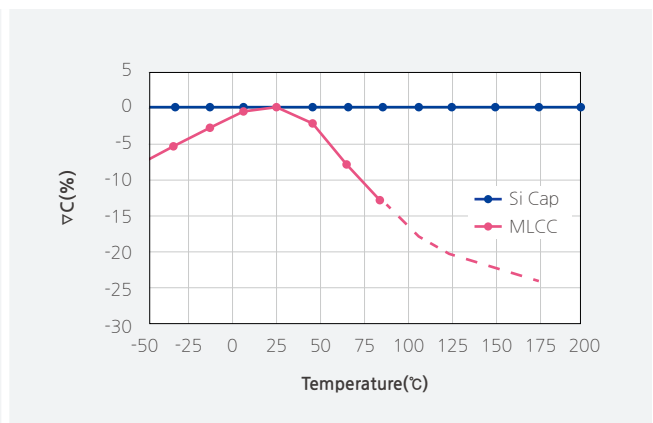
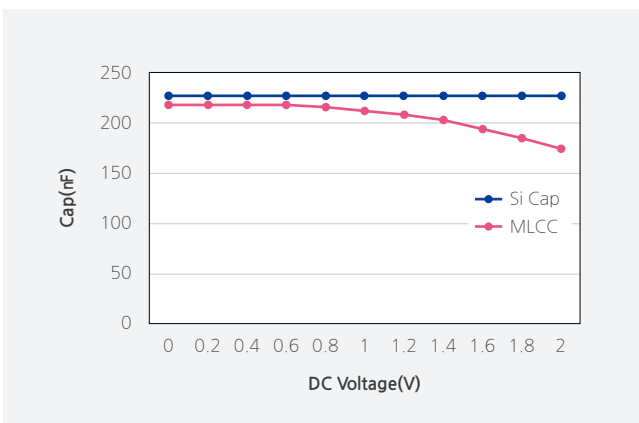
· **Low ESL**

Based on customer requirements, the number and arrangement of terminals can be optimized. This allows for the cancellation of magnetic flux, reduction of current loops, and implementation of Low ESL.

Item	Structure	ESL	Magnetic Flux Cancellation	Current Loop
MLCC		60~80pH		
Silicon Capacitor		2 ↓		

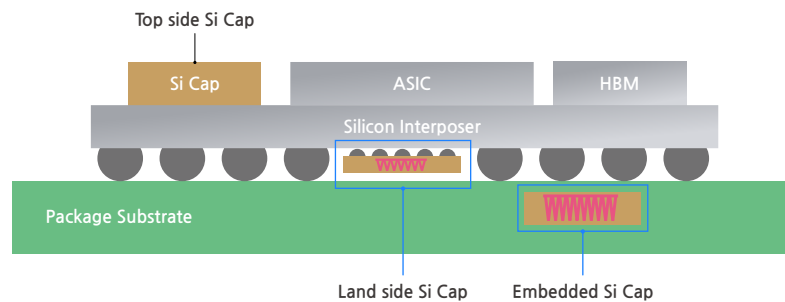
· **Low capacitance change rate**

Silicon capacitors have low capacitance change rate with DC-bias and temperature changes due to the properties of the dielectric material.



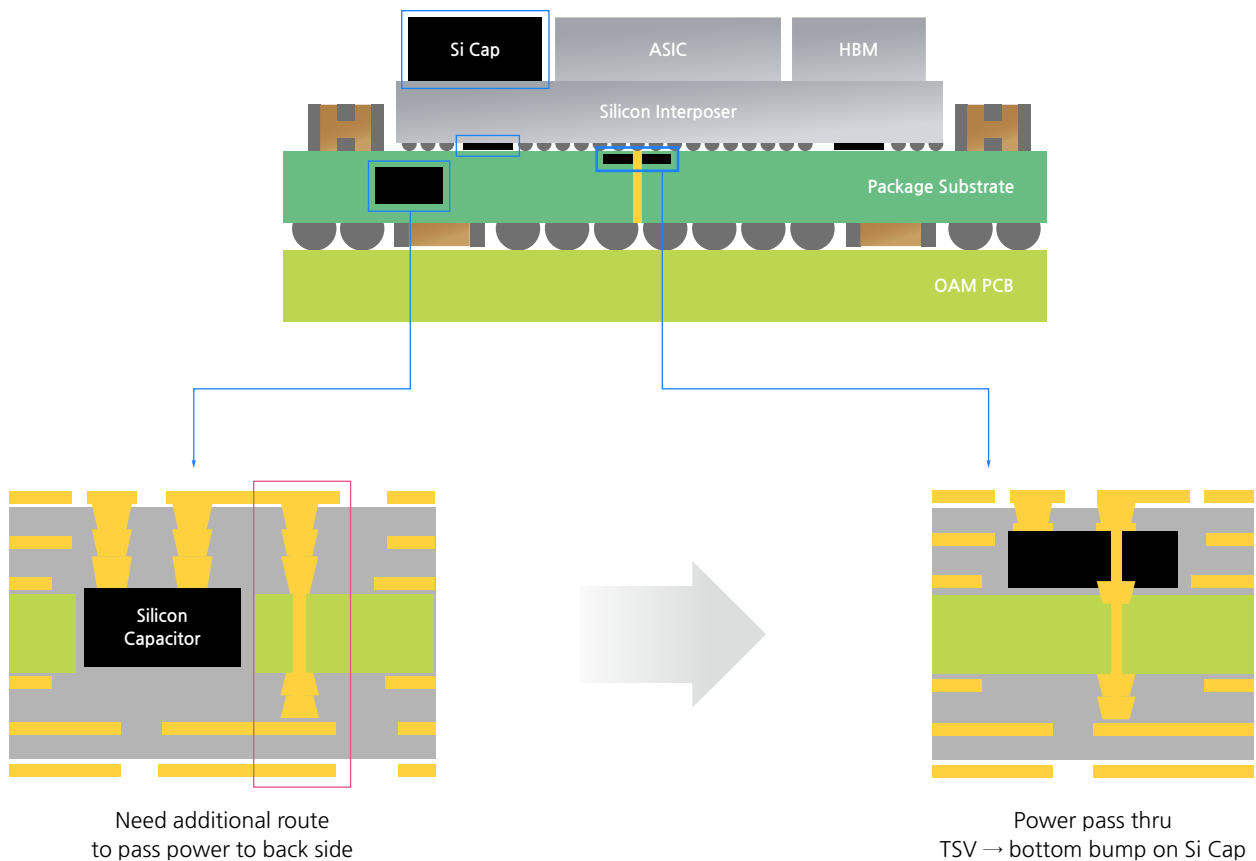
Explanation of Silicon Capacitors

- The package type and thickness of the Silicon capacitor are determined by the mounting location.
 - **Land-side Silicon capacitors:** Mounted on the bottom of the silicon interposer.
 - **Top-side Silicon capacitors:** Mounted on the side of the GPU, CPU, or ASIC.
 - **Embedded Silicon capacitors:** Embedded inside the package substrate.



* Embedded Silicon capacitor with TSV (through silicon via) in the build-up layer.

: The Silicon capacitor and power pass-through can be integrated into a single die, and it can be embedded in the build-up layer to maximize its performance. This significantly improves routing efficiency, eliminating the need for additional power rails or split cavities.



Application Guide

- Silicon capacitors were first adopted in high-performance application processors that require large capacitance and low ESL, and demand is increasing as the performance of chipsets for AI servers and automotive ADAS continues to improve.

	IT (AP)	Industry (AI server)	Automotive
Trend	high-performance, highly integrated AP	GPU performance improvement and high-speed signal connectivity with HBM	Advanced ADAS(Lv.4 ↑) and improved Processor performance.
Needs	thin form-factor, Low ESL, size reduction	ultra-high capacitance, Low ESL	high capacitance, Low ESL, High voltage High reliability (AEC-Q100 certification)
Size	1.2×1.0mm ↓	Various Size by customer (1×1mm ↓, Array-Type etc. Customized)	Various Size by customer (0.6×0.6mm ↑, Customized)
Cap. Density	2~3uF/mm ²	2~3uF/mm ²	0.5uF/mm ² ↑
ESL/ESR	2pH ↓ /4mΩ	3pH ↓ /5mΩ	3pH ↓ /5mΩ
Voltage	1.35V	1.35V~1.8V	1.35~2.5V
Thickness * Si-body	70um (LSC type) 700~800um (Embedded)	70um (LSC/DSC type) 700~800um (Embedded)	50~70um (LSC/DSC type) * Land Side Capacitor/ Die side Capacitor
PKG type	LSC(PCB), Embedded	LSC/DSC(PCB), Embedded	LSC (PCB, Si-interposer)/DSC Wire bonding/Cu Pillar

Characteristics Performance

■ Specifications can be modified according to customer requirements.

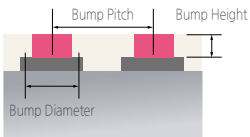
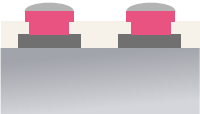

Symbol	Parameter	Conditions	Unit	Spec
C	Capacitance Value	@25°C	nF	Customized
ΔC_p	Capacitance Tolerance	@25°C	%	±20
T_{op}	Operating Temperature		°C	-40 ~ 125
T_{STG}	Storage Temperature		°C	-55 ~ 150
ΔC_T	Capacitance Temperature Variation	-40°C ~ 125°C	ppm/°C	1000
$R_{V_{DC}}$	Rated Voltage		VDC	Customized
BDV	Breakdown Voltage	@25°C	VDC	Customized
ΔC_{RVDC}	DC Capacitance Voltage Variation	0V ~ $R_{V_{DC}}$, @25°C	%/VDC	10
IR	Insulation Resistance	$R_{V_{DC}}$, @25°C, 120s	GΩ	10
ESR	Equivalent Series Resistance	@25°C, SRF	mΩ	TBD
ESL	Equivalent Series Inductance	@25°C, 1GHz	pH	TBD

Product Lineup

Part number	Size [mm]	Si thickness [μm]	Capacitance [nF]	Power rails [ea]	Rated Voltage [V]	BDV [V]	PKG	Pad size [μm]
SCBCAP305L95EGNNWT	1.26×1.03	200	3,000	4	1.2	3.7	LSC	60
SCBCAP105L95AGNNNT		65	1,000	4	1.35	4.0	LSC	60
SCBCAP514L95AGNNNT		70	512	4	1.35	4.0	LSC	60
SCBC5P254L95AGNNNT	1.26×0.51	70	256	2	1.35	4.0	LSC	60
SCG98P105M86AGNNWT	0.96×0.88	60	1,050	2	1.35	4.0	LSC	55
SCHVSP107MH1AGB9WT	11.01×8.35	750	103,950	198	1.35	4.0	DSC	55
SCRLLC885MG5EGNNWT	2.00×2.00	750	8,800	2	1.2	4.0	Embedded	200
SCRNKC166MG5EGNNWT	4.06×2.00	750	17,600	4	1.2	4.0	Embedded	200
SCRNNC326MG5EGNNWT	4.02×4.02	750	35,000	4	1.2	4.0	Embedded	200

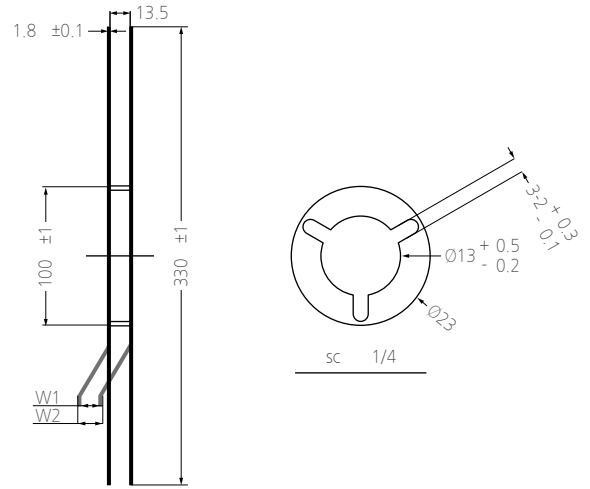
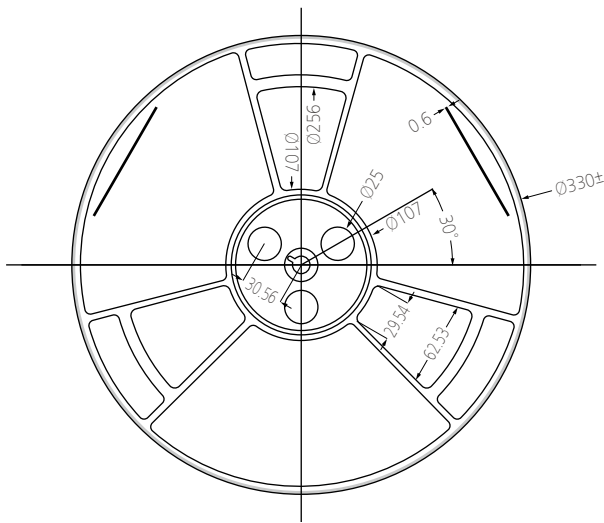
Pad and Bump Specifications

- Support customized design (SMD, Embedded, Wire bonding)
- Bump dimension (If not included in the design rule guide, consultation is required)

Specifications		Embedded type	SMD type	Wire bonding
Min. Pitch	70μm	 <p>Cu Pad</p>	 <p>Cu Pillar Bump</p>	 <p>Au/Al Pad</p>
Min. Diameter	45μm			
Height	10μm			

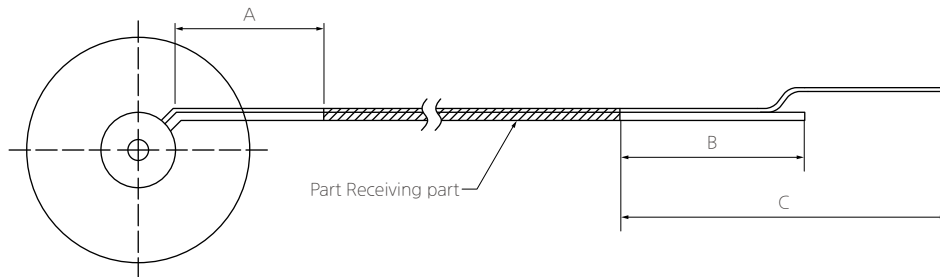
Packaging Specifications

1 Lok Reel Size



(Unit : mm)

Tape Width	Outer Diameter	Inner Diameter	W1	W2	Hall Pitch	Hall Diameter
8	330 (13")	100	9.5	13.5	30.56	Φ25

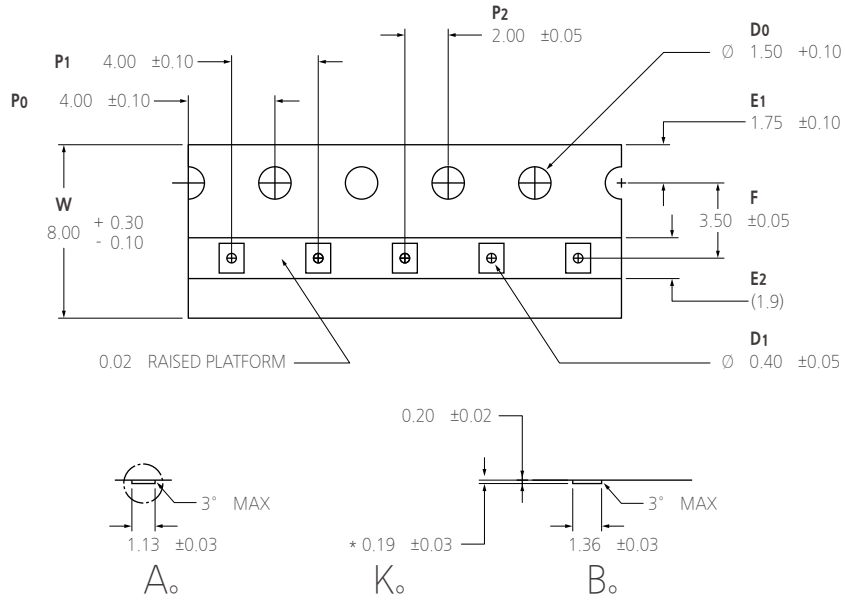


(Unit : mm)

A	B	C
1.2±0.1	1.2±0.1	1.5±0.1

Packaging Specifications

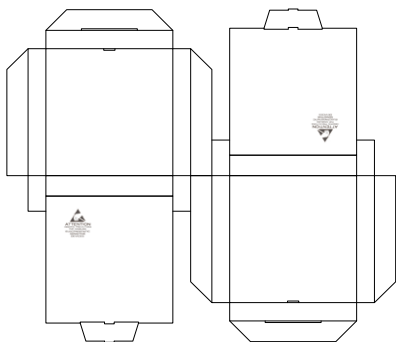
2 Tape Size



(Unit : mm)

Cavity dimension			W	P0	P1	P2	D0	D1	E1	E2	F
A0	B0	K0									
1.13±0.03	1.36±0.03	0.19±0.03	8+0.3/-0.1	4±0.1	4±0.1	2±0.05	∅1.5±0.1	∅0.4±0.05	1.75±0.1	(1.9)	3.5±0.05

3 Box Size



TOP			
		BOTTOM	

(Unit : mm)

(Unit : mm)

Inner Box (13" × 1 Reel)		
Width	Depth	Height
350	347	50

Out Box (13" × 6 Inner Box)		
Width	Depth	Height
380	370	375

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